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HARNESS, DICKEY & PIERCE, P.L.C.
P.O. BOX 8910
RESTON, VA 20195

EXAMINER	
ENGLUND, TERRY LEE	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/761,239	CHOI, JONG-HYUN	
	Examiner	Art Unit	
	Terry L. Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-13,15-33 and 35-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-3* is/are allowed.

6)☒ Claim(s) *5-13, 15-26, 29-33, and 35-37* is/are rejected.

7)☒ Claim(s) *27 and 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment/Drawings

The amendment submitted on May 26, 2006, including page 15 that indicates replacement sheets of the drawings for Figs. 5 and 8, were reviewed and considered with the following results:

Although page 15 indicates that drawings sheets for Figs. 5 and 8 were submitted as replacement sheets, those figures were not found by this examiner. Until those figures can be reviewed, their changes will not be approved. Therefore, the drawing objections described in the previous Office Action are maintained, and repeated below under the appropriate section.

The objection to the title described on page 3 of the previous Office Action was not addressed, and that objection is maintained and repeated later.

Until the corrected Fig. 5 can be reviewed, the objection to page 13, line 6 of paragraph 0036 will be maintained. However, if Fig. 5 did have an error in labeling, and it is corrected by a Replacement Sheet that can be verified, the disclosure's objection will be withdrawn. In the meantime, that objection is repeated below under its appropriate section.

It is still believed page 16, line 1 of paragraph 0043 is incorrect. Therefore, that objection is maintained, and repeated later. Comments with respect to the applicant's remarks are described later under the Response to Arguments/Comments section.

After reconsidering the original disclosure, and the applicant's comments on page 17 of the amendment, the objection to lines 6-8 of paragraph 48 on page 19 has been withdrawn.

The amended paragraphs overcame all the other objections to the disclosure described on page 3 of the previous Office Action. Therefore, those objections have been withdrawn.

However, when paragraph 0028 was reviewed, another inadvertent error was found that had been initially overlooked by the examiner. That objection is described later under the Specification section.

The renumbering of the last three active claims overcame the previous Office Action's objections to claims 34-36. Therefore, those claim objections have been withdrawn. However, when all the active claims were carefully reviewed, a few other objections were noted. These claim objections are described later under the appropriate section.

Claims 4, 14, and 34 have been cancelled. The allowable material from claims 4 and 14, as described in the previous Office Action on pages 9-10, were added to their respective independent claim (i.e. 1 and 10). The rejection of claim 34 has been rendered moot.

After reconsidering the claim language, figures, and the applicant's comments, the rejections of claims 5, 8, and 15, with a respect to the "connection node of the second and third MOS transistors" have been withdrawn. The node connection could be taken between the first and third transistors (as shown within the figures), or between the second and third MOS transistors, wherein it is understood the latter node connection will provide a lower voltage than the connection between the first and third transistors.

Although the comments on page 18 appear to indicate claims 6 and 9 were amended to overcome their rejections, those claims were not amended. Therefore, their rejections described in the previous Office Action have been maintained, and are described later.

The amended change to claim 10 basically overcame its rejections under 35 U.S.C. 112 as described on page 4 of the previous Office Action, but the amended change created a new problem described later under the appropriate section.

The comments with respect to claims 16, 25, and 31 were considered, but not found persuasive. Therefore, those claim rejections have been maintained, and are described later, along with some comments, within their respective section.

Amended claims 21 and 23 overcame their rejections with respect to "second low voltage", which have now been withdrawn.

Amended claim 30 basically overcame its rejection under 35 U.S.C. 112 described in the previous Office Action. However, the amended change still created problems that are described later under the appropriate section.

The rejection of claim 29 on page 6 of the previous Office Action was not addressed or corrected. Therefore, that rejection has been maintained, and is repeated later.

Amended independent claims 1, 10, and 32 overcame the prior art rejections of claims 1-3, 10-13, 32-33, and 35-37 under 35 U.S.C. 102(e), with respect to Hardee. Hardee lacks the second MOS transistor being controlled by a row address signal in a memory device, as now recited within each of those independent claims.

The applicant's arguments with respect to the rejections of claims 19-26 under 35 U.S.C. 102(e), with respect to Wright, were not persuasive. Therefore, these rejections (with some modifications to account for the amended changes) are described later under the appropriate section. Related comments are described under the Response to Arguments/Comments section.

The amended claims also created some new rejections under 35 U.S.C. 112, which are described later under their appropriate section.

Drawings

The drawings remain objected to because the three memory blocks labeled with "MB0" in Fig. 5 should be re-identified as --MB0--, --MB1--, and --MBy-- as cited on page 13, lines 1-2. Fig. 8 should have the information within parenthesis behind "ND22" of Fig. 8 either clarified, or removed from the figure. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The title "Semiconductor Integrated Circuit Device" of the invention is still not considered descriptive since it is generic in nature. Therefore, a new title is still required that is clearly indicative of the invention to which the claims are directed. For example, the following title is suggested: --Level shifting circuit with thick and thin gate MOS transistors--.

The disclosure remains objected to because of the following informalities: Page 13, line 6 of paragraph 0036 "DRA1k[0:x} should be --DRA1y[0:x]-- to correspond to the labeling of the original figures. Page 16, line 1 of paragraph 0043 "DRA0k" should be --DRAk0-- since that is the signal clearly shown being applied to the input of logic gate G20, which controls the on/off operations of transistors MN22 and MN23.

The disclosure is also objected to because of the following informality previously overlooked, but found when the amended paragraphs were reconsidered. On page 2 of the amendment, line 6 of paragraph 0028 should have --MN3-- instead of "MN4", since MN3 is the transistor that is understood to be always in the turn-on state.

Appropriate corrections are required with respect to the objections described above.

Claim Objections

Claims 19-31 are objected to because of the following informalities: To minimize possible confusion with respect to a "node having a relatively thin gate insulation layer" now recited within claim 19, it is suggested a comma be added after "transistor" on both lines 6 and 7, after "a third internal node" on line 6, and after "node" on line 9. These changes will then provide a clearer relationship between the layer and its respective MOS transistor. Claim 29, line 10 "have" should be --has-- to correspond with its associated term "each." Each of claims 20-31 carry over the objection from claim 19, and each of claims 30-31 also carry over the objection from claim 29. Appropriate corrections are required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 6, 8, 10-13, 17-18, and 25-31 remain rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. It is not clear how "a voltage higher than the power supply voltage" within each of claims 6 and 9 relates to "a first voltage higher than a power supply voltage" as recited within claim 1. Since the power terminal of claim 10 now receives "a high voltage", how does that relate to the first transistor's source being coupled to "the first high voltage"? It is not clear how "a voltage higher than the power supply voltage" within claim 16 relates to "a high voltage that is higher than a power supply voltage" as recited within claim 10, or to its "the first high voltage." It is still believed claim 25, line 1 "the first MOS transistor" is misleading, and/or inaccurate. Was --the fifth MOS transistor-- meant instead? [Using the applicant's Fig. 4 as an example, fifth/sixth transistors MN11/MN12 are controlled by an inverted input signal with respect to one another, wherein first transistor MP5 is controlled by the voltage on node ND3.] Since claim 29 indicates each row decoder and driver circuit includes a fifth internal node, it is not clear in claim 30 if only a single inverter is coupled to each one of those fifth internal nodes from claim 29, or if a corresponding inverter is coupled to its own respective fifth internal node. Similarly, which "word line" does the "inverter" actually drive, since each row decoder/driver circuit has its own corresponding word line? It is not clear how "a voltage higher than the power supply voltage" within claim 31 relates to "a high voltage higher than a power supply voltage" as now recited within claim 19.

Claim 29 still recites the limitation "the row decoder and driver block" in line 2 with insufficient antecedent basis for this limitation in the claim. Was claim 29 meant to depend on claim 28?

Claims 5-9, 15-16, 18, 32-33, and 35-37 are now rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 5 and 15 each now depend on a cancelled claim. It is not clear in claim 7 how "a third MOS transistor", "a relatively thick gate insulation layer", and "a row address signal in a memory device" relate to "a third MOS transistor", "a relatively thin gate insulation layer", and "a row address signal in a memory device" now recited within claim 1. It is not understood how "a memory device" of claim 18 relates to "a memory device" now recited within claim 10. For example, do they refer to the same device, or distinct devices? The use of second and third MOS transistors within claim 32 implies a first MOS transistor that is not clearly described within the claim. Also, how can the third MOS transistor can operate "at the second voltage" is it might already be operating at the first voltage (e.g. see "operating at one of the first voltage and second voltage") as lines 8-10 of claim 32 appear to indicate can happen? Although claim 34 was cancelled, amended claims 36-37 indicate they depend on "claim 32." However, the change from the previous dependency on "claim 34" to the now recited "claim 32" has not been identified within the amended claims. Therefore, it is not clear what claim language within claims 36-37 is actually intended.

Dependent claims carry over any rejection(s) from any claim(s) upon which they depend.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 19-26 remain rejected under 35 U.S.C. 102(e) as being anticipated by Wright et al. (Wright), a reference cited in the previous Office Action. Fig. 2 shows a semiconductor integrated circuit device comprising power terminal 222 receiving high voltage VIO that is higher than power supply voltage VCORE of the device (e.g. see column 3, lines 48-57); first MOS transistor 210; second MOS transistor 212, third MOS transistor 206; fourth MOS transistor 208; fifth MOS transistor 202; sixth MOS transistor 204; and ground voltage 226. Since the basic structure in Fig. 2 closely corresponds to the applicant's own Fig. 4 circuit, and since Wright's Fig. 2 does not label all the internal nodes, one of ordinary skill in the art would still know the device also comprises the first-fourth internal nodes. Wright discloses first/second MOS transistors 210/212 have a thick gate oxide; fifth/sixth MOS transistors 202/204 have a thin gate oxide; and third/fourth MOS transistors 206/208 can have a medium gate oxide (e.g. see column 4, lines 17-27). Since transistors with a medium gate oxide have relatively thin gate insulation layers with respect to those transistors with a thick gate oxide, claims 19-20 are anticipated. Power supply voltage VCORE is an internal power supply voltage of the device

(e.g. see column 3, lines 49-50), anticipating claim 21. First MOS transistor 210 is controlled by a voltage of the second internal node (i.e. the node between 212 and 208), and second MOS transistor 212 is controlled by a voltage of the first internal node (i.e. the node between 210 and 206), anticipating claim 22. The gates of third/fourth MOS transistors 206/208 are coupled to low voltage VCORE, which is lower than high voltage VIO, thus anticipating claim 23. Power supply voltage VCORE is an internal power supply voltage of the device (e.g. see column 3, lines 49-50), and it is lower than power supply voltage VIO, anticipating claim 24. Fifth/sixth transistors 202/204 are controlled by first input signal VIN and its inverted version (via inverter 214), respectively, thus anticipating claim 25. It is understood that first input signal VIN, and its inverted version, are selectable to have one of a high level of low voltage VCORE and a low level of ground (e.g. see column 3, lines 48-50; and the connection of inverter 214 between VCORE and ground), anticipating claim 26.

Allowable Subject Matter

Claims 1-3 are allowed. There is presently no motivation to modify or combine any prior art reference(s) to ensure the second MOS transistor is controlled by a row address signal in a memory device.

Claims 27-28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. There is presently no motivation to modify or combine any prior art reference(s) to ensure the first input signal includes a row address signal, and a block selecting signal, from a memory device as recited within claim 27, upon which claim 28 depends.

Claims 10 and 32 would be allowable if satisfactorily rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action. There is presently no motivation to modify or combine any prior art reference(s) to ensure the second input signal includes a row address signal from a memory device as recited within claim 10, or the second MOS transistor is controlled by a row address signal in a memory device as recited within claim 32.

Claims 5-9, 11-13, 15-18, 29-31, 33, and 35-37 would be also allowable if satisfactorily rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. Each of these dependent claims apparently depend on one of the independent claims described above (i.e. 1, 10, or 32).

Response to Arguments/Comments

The applicant's arguments filed May 26, 2006 have been fully considered but they are not persuasive with respect to the specification correctly referring to "decoding signal DRA0k" shown in Fig. 5; the "voltage higher than the power supply" recited within claim 16; or the control of the first/sixth transistors as recited within claim 25. For example, the on/off operations of transistors MN22 and MN23 are controlled by output NOUT of logic gate G20, which is clearly shown receiving input signals DRAk0 and BLK0, wherein each of those signals has levels of IVC/EVC. If "decoding signal DRA0k" was actually meant on line 1 of paragraph 0043, that would be objected to also for several reasons. The output of the level shift block shown in Fig. 5 is signal "DRA0k0", not "DRA0k", and it has a level of VPP. How would this level shifted output turn transistors MN22 and MN23 on/off as the applicant apparently implies?

Although the transistors of claim 16 can operate at a voltage higher than the power supply voltage, the claim still does not describe how that voltage relates to the voltages cited in claim 10. Therefore, that rejection was maintained. Since claim 19 provide a fairly specific arrangement of the first-sixth MOS transistors, it is still believed the limitations recited within claim 25 are misleading. Therefore, it is requested the applicant's submit an appendix (or some type of thorough explanation) clearly showing/describing how the structure cited in claim 19, along with the first MOS transistor being controlled by a first input signal, and the sixth MOS transistor being controlled by an inverted version of the first transistor, will function. Although the examiner is not attempting to limit the applicant to only the figures shown, what is actually being claimed should be clearly supported by the original disclosure so one reviewing the application can discern what is feasible, and what may not have been disclosed clearly, and is therefore questionable.

The applicant's arguments also fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references with respect to the rejections of claims 19-26 under 35 U.S.C. 102(e) and the reference of Wright et al. Since Wright clearly discloses transistors 206 and 208 can have either thick or medium layers (e.g. see column 4, lines 17-19), when they are medium, one of ordinary skill in the art will understand the layers will be relatively thin with respect to the thick layers of transistors 210 and 212. For example, one of ordinary skill in the art would know that if a circuit comprises various transistors having either thick, medium, or thin insulation layers, the transistors having medium layers will have layers that are (relatively) thinner than those of transistors having thick layers,

and transistors having thin layers will have layers that are thinner than the transistors having either the medium and thick layers. The Wright reference (again see column 4, lines 17-19), and basic understanding of the concept of thick, medium, and thin, do not require the examiner to cite an additional reference to make this rejection as the applicant apparently demands. Since Wright clearly discloses that transistors 210 and 212 have thick gate oxides, and transistors 206 and 208 can have either thick or medium gate oxides, what prevents transistors 206 and 208 from having the medium gate oxides as disclosed by Wright? Is the applicant implying that a medium gate oxide layer is either equal to, or perhaps even larger than, a thick gate oxide layer when a circuit has at least two transistors, with one having a medium layer, and the other having a thick layer?

Therefore, the rejections described in this Office Action, as well as the previous Office Action, are deemed proper with respect to the broadest reasonable interpretation of the claimed limitations, and of the prior art references.

Prior Art

The prior art on the accompanying PTO-892 is cited for interest. Fig. 1 of Clark et al. shows transistor 150, 140, and 130 coupled in series between high voltage 180 and ground, wherein transistor 150 has a thick layer, and transistors 130 and 140 have thin layers (see column 2, line 66 to column 3, line 9). Clark discloses address lines on column 5, lines 41-43. Therefore, this reference should be reviewed and considered with respect to at least the basic limitations of the claims.

The applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE

Terry L. Englund

28 July 2006

QUAN TRA
PRIMARY EXAMINER